



## **Extreme DA Collaborates with Japan's STARC to Develop New-Generation Analysis Flow for IC Design**

*ICs Designed at the 65-nm and 45-nm Process Nodes Demand a New-Generation Statistical Approach for Faster, Higher-quality Production*

**Palo Alto, Calif.** — May 15, 2007 — Extreme DA™ and Japan's leading semiconductor technology research organization—Semiconductor Technology Academic Research Center (STARC)—are collaborating to jointly develop and validate a variability-aware timing analysis flow for integrated circuits (ICs) manufactured in 65- and 45-nanometer (nm) processes. The flow features Extreme XT™ for statistical static timing analysis (SSTA), which provides performance and power optimization in conjunction with common IC design toolsets. Extreme DA is the emerging leader in advanced timing analysis software that improves parametric yield and addresses the many process variations in the latest generation of semiconductors.

At advanced process nodes of 65-nm and below, statistical analysis software is required for analyzing device mismatch and global variations. This analysis helps designers understand the impact these effects have on meeting timing targets for their IC designs. STARC has established the correlation between the Extreme XT timing analyzer and SPICE for 65-nm designs, and verified Extreme XT's suitability for the statistical optimization of designs.

"We are committed to analyzing, testing, and delivering advanced tool flows to meet critical issues in manufacturing-aware design," said Nobuyuki Nishiguchi, vice-president and general manager of Development Department-1 at STARC. "Working with innovative and emerging technology leaders like Extreme DA and bringing verified flows to our member companies is a key mission for STARC. The Extreme DA technology is at the leading edge for statistical timing analysis."

"In Japan, STARC is the leader in investigating advanced methodologies and delivering them to its member companies," said Mustafa Celik, president and CEO of Extreme DA. "I am pleased we are working closely with STARC to validate our leading statistical timing analysis. We believe the collaboration will result in increased adoption of our signoff timing solution by makers of advanced IC designs."

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**About STARC**

The Semiconductor Technology Academic Research Center (STARC) of Yokohama, Japan, is a research consortium co-founded on December 28, 1995 by major Japanese semiconductor companies. STARC's mission is to contribute to the growth of the Japanese semiconductor industry by developing leading edge System-on-Chip (SoC) design technologies.

STARC shareholders are Fujitsu Limited, Matsushita Electric Industrial Co., Ltd., NEC Electronics Corporation, Oki Electric Industry Co., Ltd., Renesas Technology Corporation, Rohm Co., Ltd., Sanyo Semiconductor Co., Ltd., Seiko Epson Corporation, Sharp Corporation, Sony Corporation, and Toshiba Corporation. For more information about STARC, please visit [www.starc.jp](http://www.starc.jp).

**About Extreme DA**

Headquartered in Palo Alto, Calif., venture-funded Extreme DA develops and licenses software products for SoC timing signoff of 65- and 45-nanometer integrated circuits. The company's investors include Foundation Capital, IT-Farm Corporation, and Lanza techVentures. For the latest news and information on Extreme DA, visit [www.extreme-da.com](http://www.extreme-da.com) or write to [info@extreme-da.com](mailto:info@extreme-da.com).

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